1. A method of erasing the reference cells in a flash EPROM memory in an integrated circuit whereby said erasing is initiated by a pulse generated upon each application of supply voltage to said flash EPROM.

2. The method according to Claim 1 whereby said pulse has duration of between about 0.1 and 10mS.

3. The method according to Claim 2 whereby said duration of said pulse is determined by the values of one capacitor and one resistor.

4. The method according to Claim 3 whereby said capacitor is a MOSFET device.

5. The method according to Claim 3 whereby said resistor is a MOSFET device.

6. The method according to Claim 1 whereby said pulse is generated by a power on reset circuit comprised of:

a first capacitor with one terminal grounded and the other terminal is connected to a first node;

a first resistor with a one terminal tied to $V_{DD}$ and the other terminal tied to said first node;

a plurality of inverters where the input of said plurality of said inverters is connected to said first node and the output of said plurality of inverters is connected to the circuit output;

a latch comprised of a first and second inverter where the input of said first inverter and the output of said second inverter are connected to said first node and the input of said second inverter and the output of said first inverter are connected to a second node;

a second capacitor with one terminal connected to $V_{DD}$ and the other terminal connected to said second node;

a first MOSFET with the drain terminal connected to said second node, the source terminal connected to ground and the gate terminal connected to a third node;

a second resistor with one terminal connected to said third node and the other terminal connected to ground;

a third resistor with one terminal connected to said third node and the other terminal connected to a fourth node; and

a second MOSFET with the drain terminal connected to $V_{DD}$, the source terminal connected to said fourth node and the gate terminal connected to said circuit output.

7. The method according to Claim 6 whereby said first capacitor is a MOSFET device.

8. The method according to Claim 6 whereby said second capacitor is a MOSFET device.

9. The method according to Claim 6 whereby said first resistor is a MOSFET device.

10. A method of erasing the reference cells in a flash EPROM memory in an integrated circuit whereby said erasing is initiated by a pulse generated of duration between about 0.1 and 10mS upon each application of supply voltage to said flash EPROM.

11. The method according to Claim 10 whereby said duration of said pulse is determined by the values of one capacitor and one resistor.

12. The method according to Claim 11 whereby said capacitor is a MOSFET device.

13. The method according to Claim 11 whereby said resistor is a MOSFET device.

14. The method according to Claim 10 whereby said pulse is generated by a power on reset circuit comprised of:

a first capacitor with one terminal grounded and the other terminal is connected to a first node;

a first resistor with a one terminal tied to $V_{DD}$ and the other terminal tied to said first node;

a plurality of inverters where the input of said plurality of said inverters is connected to said first node and the output of said plurality of inverters is connected to the circuit output;

a latch comprised of a first and second inverter where the input of said first inverter and the output of said second inverter are connected to said first node and the input of said second inverter and the output of said first inverter are connected to a second node;

a second capacitor with one terminal connected to $V_{DD}$ and the other terminal connected to said second node;

a first MOSFET with the drain terminal connected to said second node, the source terminal connected to ground and the gate terminal connected to a third node;

a second resistor with one terminal connected to said third node and the other terminal connected to ground;

a third resistor with one terminal connected to said third node and the other terminal connected to a fourth node; and

a second MOSFET with the drain terminal connected to $V_{DD}$, the source terminal connected to said fourth node and the gate terminal connected to said circuit output.

15. The method according to Claim 14 whereby said first capacitor is a MOSFET device.

16. The method according to Claim 14 whereby said second capacitor is a MOSFET device.

17. The method according to Claim 14 whereby said first resistor is a MOSFET device.

18. A method of erasing the reference cells in a flash EPROM memory in an integrated circuit whereby said erasing is initiated by a pulse generated of duration between about 0.1 and 10mS upon each application of supply voltage to said flash EPROM, wherein said pulse is generated by a power on reset circuit comprised of:

a first capacitor with one terminal grounded and the other terminal is connected to a first node;

a first resistor with a one terminal tied to $V_{DD}$ and the other terminal tied to said first node;

a plurality of inverters where the input of said plurality of said inverters is connected to said first node and the output of said plurality of inverters is connected to the circuit output;

a latch comprised of a first and second inverter where the input of said first inverter and the output of said second inverter are connected to said first node and the input of said second inverter and the output of said first inverter are connected to a second node;

a second capacitor with one terminal connected to $V_{DD}$ and the other terminal connected to said second node;

a first MOSFET with the drain terminal connected to said second node, the source terminal connected to ground and the gate terminal connected to a third node;

a second resistor with one terminal connected to said third node and the other terminal connected to ground;

a third resistor with one terminal connected to said third node and the other terminal connected to a fourth node; and

a second MOSFET with the drain terminal connected to $V_{DD}$, the source terminal connected to said fourth node and the gate terminal connected to said circuit output;

and wherein said duration of said pulse is determined by the values of said first capacitor and said first resistor.

19. The method according to Claim 18 whereby said first capacitor is a MOSFET device.

20. The method according to Claim 18 whereby said second capacitor is a MOSFET device.

21. The method according to Claim 18 whereby said first resistor is a MOSFET device.